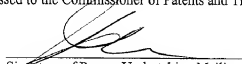


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Date: September 29, 2000

Sir:

Transmitted herewith for filing is the patent application of Minoru NAKANO, Masaaki UENO, and Kazuo TANAKA  
(Name of Inventor)

**FOR: METHOD AND APPARATUS FOR CONTROLLING A SEMICONDUCTOR FABRICATION  
TEMPERATURE**  
(Title of Application)

## ENCLOSED ARE:

- (x) **Specification** (25 pages), Claims (4 pages/14 claims) & **Abstract**: Yes X; 8 Sheets of Drawings - Figs. 1-9;  
(x) **Declaration and Power of Attorney** EXECUTED? Yes X  
(x) **Assignment to Kokusai Electric Co., Ltd.**, 14-20, 3-chome, Higashi-Nakano, Nakano-ku, Tokyo, Japan 164-8511  
Certified copy of Japanese Patent Appln. No. 2000-019934 filed on January 28, 2000  
the priority of which is claimed under 35 USC 119;  
( ) Verified Statement to establish **Small Entity Status** under 37 CFR 1.9 and 1.27  
( ) Information Disclosure Statement, PTO-1449 and references;

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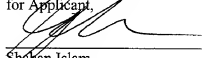
	Claims filed	Extra	SMALL ENTITY or LARGE ENTITY	
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Indep. Claims	1-3	0	\$	\$
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METHOD AND APPARATUS FOR CONTROLLING  
A SEMICONDUCTOR FABRICATION TEMPERATURE

Field of the Invention

The present invention relates to a semiconductor manufacturing method and apparatus; and, more particularly, to a method and apparatus for use in controlling processing temperatures during the fabrication of semiconductor devices.

Background of the Invention

In a conventional single wafer epitaxial growth apparatus for processing substrates such as silicon wafers one at a time, a substrate is loaded into a processing chamber of the growth apparatus and heated upto a predetermined processing temperature while supplying reaction gases to form a thin film on top of the substrate.

In such a single wafer epitaxial growth apparatus, it is crucial to control temperatures inside the processing chamber appropriately. In detail, temperature uniformity throughout a wafer is required during maintaining a constant temperature of the wafer and also during heating/cooling processes thereof; and the accuracy of the temperature control greatly affects the quality of a semiconductor device to be manufactured. The temperature uniformity

throughout the wafer surface in such a single wafer epitaxial growth apparatus is more crucial than in a batch-type thermal processing apparatus such as a vertical-type thermal diffusion furnace.

5           One of conventional techniques for controlling uniform temperatures inside a thermal processing chamber is described in a Japanese Patent Laid-Open Publication No. 64-8225. According to the prior art reference above, the processing chamber is provided with electric heaters for  
10   heating a center portion and an edge portion of a body to be heated and the heaters are controlled based on the differences between a target temperature and actual temperatures of the body measured by employing a temperature sensor. In the conventional method, a power fed to an  
15   electric heater for heating the edge portion of the body is kept to be less than that provided to an electric heater for heating the center portion.

Since, however, the conventional temperature control method described above does not provide the temperature  
20   uniformity during the heating/cooling processes, which is strictly required in the single wafer epitaxial growth apparatus, the conventional method may not be suitably employed therein to obtain the desired temperature uniformity which in turn gives rise to a required device  
25   quality.

Further, it is not desirable to install a number of

temperature sensors in the single wafer epitaxial growth apparatus and monitor temperatures at various regions of a wafer during a process in order to control processing temperatures since the installation of the temperature sensors itself might cause contamination problems during the process due to substances which can be generated therefrom.

Accordingly, it is needed to accomplish the required temperature uniformity over a wafer in the single wafer epitaxial growth apparatus without measuring temperatures at various regions of the wafer during a process.

#### Summary of the Invention

It is, therefore, a primary object of the present invention to provide a method for controlling temperatures in a semiconductor manufacturing apparatus to achieve the desired temperature uniformity over a semiconductor substrate to thereby improve the quality of a semiconductor device fabricated. In accordance with the present invention, temperature uniformity throughout the substrate is provided over any preset temperature range by simply monitoring temperatures at one or two predetermined locations in a processing chamber of the semiconductor manufacturing apparatus without monitoring the temperatures at various regions of the substrate.

Another object of the present invention is to provide

a semiconductor manufacturing apparatus employing the inventive temperature control method described.

Still another object of the invention is to provide a semiconductor manufacturing method employing the inventive temperature control method.

In accordance with one aspect of the present invention, there is provided a method for controlling temperatures in a semiconductor manufacturing apparatus including a reaction chamber and a plurality of heating sources, comprising the steps of:

determining a set of power ratios to be fed to the heating sources for each of two or more selected temperatures; and

controlling a given temperature by performing power control on the heating sources based on at least one set of power ratios obtained in the determining step.

In accordance with another aspect of the present invention, there is provided a semiconductor device manufacturing method by using the temperature controlling method described above.

In accordance with still another aspect of the present invention, there is provided a temperature controlling apparatus by using the temperature controlling method described above.

In accordance with still another aspect of the present invention, there is provided a semiconductor manufacturing

apparatus by using the temperature controlling method described above.

When an amount of heat being generated from the heating sources is equal to that being dissipated from the processing chamber, the total amount of heat remaining therein can be maintained constant and thus an overall thermal steady-state can be maintained. Even under the overall thermal steady-state, however, temperatures can vary at different regions of a wafer being processed and at various locations of the processing chamber.

Accordingly, in order to maintain a uniform temperature over the regions dissipating varying amounts of heat therefrom, a greater power should be supplied to a heating source for heating a region dissipating more heat. Therefore, a plurality of different regions to be controlled to have a uniform temperature are set and a power ratio capable of rendering a uniform temperature at the plurality of regions is determined in advance for each of predetermined various temperatures. By using these power ratios, temperatures across the wafer can be stabilized fast within a certain temperature range even after a temperature change, e.g., due to a heating/cooling process.

Through the use of the temperature control method described above, optimum power ratios for different regions can be determined by using target temperatures or measured temperatures obtained only from selected regions, without

monitoring temperatures from all the regions to be controlled to have a uniform temperature; and, therefore, uniform temperature control over a surface of a substrate can be achieved even during a ramp-up/down process and a reaction process (e.g., deposition and etching).

#### Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with the accompanying drawings in which:

Fig. 1 illustrates a schematic side view of a processing chamber of a single wafer epitaxial growth apparatus in accordance with a preferred embodiment of the present invention;

Fig. 2 depicts a block diagram of a lamp controller in accordance with the preferred embodiment of the present invention;

Fig. 3 provides a flow chart for describing a method for controlling temperatures in accordance with a preferred embodiment of the present invention;

Fig. 4 is an exemplary power ratio table for a setting temperature of 500°C;

Fig. 5 shows an exemplary power ratio table for a setting temperature of 700°C;

Fig. 6 sets forth an exemplary target temperature profile of a wafer in accordance with a preferred embodiment of the present invention;

Fig. 7 represents temperature profiles controlled by using PID and PD-I power ratio control schemes in accordance with the preferred embodiment of the present invention;

Fig. 8 exemplifies temperature profiles controlled based on target and measured temperatures in accordance with the preferred embodiment of the present invention; and

Fig. 9 outlines an overall process for controlling temperatures inside the single wafer epitaxial growth apparatus in accordance with the preferred embodiment of the present invention.

#### Detailed Description of the Preferred Embodiments

Referring to Fig. 1, there is illustrated a schematic side view of a processing chamber 100 of a single wafer epitaxial growth apparatus in accordance with a preferred embodiment of the present invention. In the processing chamber 100, a substrate such as a silicon wafer 103 is mounted in a reaction chamber 102 and heated to a predetermined temperature; and reaction gases are supplied therinto, thereby forming a thin film on top of the wafer 103.

Heating sources are formed of two sets 104 and 105 of

circle lamps of a ring shape installed outside the reaction chamber 102, one above and the other below the reaction chamber 102. The upper and the lower sets 104 and 105 of circle lamps respectively include a multiplicity of, e.g., 13, circle lamps represented by numerals 0 to 12 and 0' to 12' in small circles as shown in Fig. 1.

Most of the heat from each circle lamp are absorbed by the wafer 103, the reaction gases supplied into the reaction chamber 102 and a susceptor (e.g., SiC susceptor) 106 of a large heat capacity for supporting the wafer 103. The circle lamps 0-8 and 9-12 of the upper set 104 of circle lamps constitute a central zone and a peripheral zone, respectively. The circle lamps 0' to 7' and 8'-12' of the lower set 105 of circle lamps constitute a central zone and a peripheral zone thereof, respectively.

A central temperature sensor 107 and a peripheral temperature sensor 108 are installed at a center portion and a periphery portion of the processing chamber 100, respectively. Upper temperature profile sensors 109 are installed at, e.g., eleven positions on a surface of the wafer 103 as indicated by A to K in Fig. 1; and lower temperature profile sensors 110 are installed at, e.g., eleven positions on a surface of the susceptor 106 as indicated by A' to K' in Fig. 1.

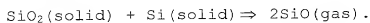
The sensors 109 and 110 are employed only during a power acquisition stage for determining power ratios to the

circle lamps 0-12 and 0'-12' in advance by measuring the temperatures at the predetermined positions, and thus are removed thereafter and are not used during an actual semiconductor processing stage, e.g., deposition and etching processes. The susceptor 106 is rotatably supported by a supporting member 111, center of the supporting member 111 functioning as a rotational axis. A fixed SiC ring die 112 is installed around the periphery of the susceptor 106. The processing chamber 100, the wafer 103, the susceptor 106, the supporting member 111 and the SiC ring die 112 have substantially circular shapes when viewed from top of the processing chamber 100.

In the processing chamber 100, there is installed the rotatable supporting member 111 at a center portion of the substrate and heat can be easily dissipated therethrough. Further, since there is a loading/unloading port (not shown) of the reaction chamber 102 at a peripheral portion thereof, heat can also be easily dissipated therethrough. It is undesirable to install many temperature sensors in view of space and contamination problems which might occur therefrom. Accordingly, by installing the temperature sensor 107 and 108 at the center portion and the peripheral portion where temperatures are unstable and by using the measured temperatures obtained therefrom in controlling processing temperatures, the number of temperature sensors can be minimized and the temperatures can be precisely controlled.

As is well known in the art, silicon becomes metallic and highly reactive at elevated temperatures to thereby readily form an oxide film on the surface thereof by the reaction with oxygen or moisture. Generally, a silicon  
5 wafer is prepared by slicing a silicon ingot, which is produced by dipping a seed crystal of silicon mounted on a rotating rod into a molten silicon contained in a quartz crucible and slowly cooling down the crystallized silicon while pulling out the rotating rod.

10 Since a silicon wafer produced in a manner described above normally has defects of about  $10^6/\text{cm}^3$  including, e.g., oxygen precipitate, voids and/or vacancies, an oxide film and such defects should be removed from the surface of the silicon wafer prior to an epitaxial growth. Accordingly, a  
15 silicon wafer is baked at a temperature of about  $1000^\circ\text{C}$  or above in a high purity hydrogen gas. The oxide is removed by the thermal reaction below:



20 Defects of the surface region of the Si wafer are removed and planarized by the high temperature reflow process and then an ideal single crystalline Si surface can be obtained. Si epitaxial growth is carried out by CVD (chemical vapor deposition) in a gaseous atmosphere composed of hydrogen gas and a Si-containing gas source, e.g.,  
25 silicon tetrachloride ( $\text{SiCl}_4$ ), trichlorosilane (TCS:  $\text{SiHCl}_3$ ), dichlorosilane (DCS:  $\text{SiH}_2\text{Cl}_2$ ) and monosilane ( $\text{SiH}_4$ ).

Fig. 2 is a block diagram of a lamp controller 20 in accordance with the preferred embodiment of the present invention. The lamp controller 20 controls powers to be supplied to the heating sources 0-12 and 0'-12' in the upper and lower sets 104 and 105 of circle lamps. The lamp controller 20 includes a CPU 201, a ROM 202 for OS and application programs, a RAM 203 for OS programs, a RAM 204 for application programs, a NVRAM 205 for OS programs, a NVRAM 206 for application programs and a device driver 207 for controlling communication control LSI circuitry.

The device driver 207 is connected to temperature monitoring units 21 to 24, a display/operation unit 25 and a lamp power output unit 26 as shown in Fig. 2. The first temperature monitoring unit 21 monitors an output of the temperature sensor 107 installed at the center portion of the processing chamber 100. The second temperature monitoring unit 22 monitors an output of the temperature sensor 108 installed at the periphery portion of the processing chamber 100. The third temperature monitoring unit 23 monitors outputs from the upper temperature profile sensors 109 for detecting temperatures of a surface of the wafer 103. The fourth temperature monitoring unit 24 monitors outputs of the lower temperature profile sensors 110 for detecting temperatures of a surface of the susceptor 106.

The lamp controller 20 reads temperatures detected

from the temperature sensors 107 and 108 via the monitoring units 21 and 22 to thereby carry out power ratio control operation by comparing the temperatures detected at the temperature sensors 107 and 108 with a predetermined target temperature. Details of the power ratio control operation will be discussed hereinafter. The result of the power ratio control operation is periodically fed to the lamp power output unit 26 as a power ratio control output value (ranging from 0% to 100%) for each circle lamp.

In response to the power ratio control output values from the lamp controller 20, the lamp power output unit 26 outputs a power for each of the circle lamps 0-12 and 0'-12' of the upper and lower sets 104 and 105. Monitored temperatures and power ratio control output values obtained are transmitted to the display/operation unit 25, enabling the real time control state to be provided to an operator.

The temperature monitoring units 21 to 24 convert analog temperature signals outputted from corresponding temperature sensors into digitized temperature signals and then send the digitized temperature signals to the lamp controller 20 through a digital communication channel. By using the digital communication channel, improved anti-noise, distortion and interference properties can be obtained in comparison with the analog communication.

Since a high speed operation is required in the monitoring units 21 and 22, the number of temperature

sensors connected to each of the monitoring units 21 and 22 is limited to one. On the other hand, the temperature monitoring units 23 and 24 are not used in control operation during an actual device processing step but instead are merely used prior to the actual processing step in order to determine proper power ratios for the circle lamps capable of obtaining a uniform temperature at a surface of a wafer. Accordingly, high speed operation is not required in the temperature monitoring units 23 and 24, and, therefore, a plurality of, e.g., eleven, temperature sensors (11 channels) are connected thereto.

Fig. 3 is a flow chart describing a method for controlling temperatures in accordance with the preferred embodiment of the present invention. At step 300, a set of power ratios for the heating sources is determined for each of predetermined setting temperatures and stored as the power ratios thereof. Power ratio determination scheme will be described in further detail hereinafter.

Next, at step 310, measured temperatures from the temperature sensors 107 and 108 are compared with predetermined target temperatures of the wafer 103; and P(proportional), I(integral), D(derivative) operation outputs are obtained with respect to the central and the peripheral zones. For example, a temperature output PV1 measured at an instant from the central temperature sensor 107 is compared with a corresponding target temperature to

provide P, I, D operation outputs of the central zone at that instant; and a temperature output PV2 obtained at that instant from the peripheral temperature sensor 108 is compared with the corresponding target temperature to generate P, I, D operation outputs of the peripheral zone at that instant. The P, I and D operation outputs determination scheme is well known in the art and, therefore, will not be described in detail for the sake of simplicity.

In the preferred embodiment shown in Fig. 1, the central zone corresponds to the regions where the circle lamps 0-8 of the upper set 104 of circle lamps and those 0'-7' of the lower set 105 of circle lamps are located. The peripheral zone corresponds to the regions where the circle lamps 9-12 of the upper set 104 of circle lamps and those 8'-12' of the lower set 105 of circle lamps are disposed.

Thereafter, at step 320, power ratio control operation is performed based on the P, I, D operation outputs obtained from step 310 and the power ratios predetermined at step 300, thereby determining a power ratio control output for each of the circle lamps of the upper and lower sets 104 and 105 of circle lamps. At the lamp power output unit 26, the power ratio control output is converted into a corresponding actual lamp power and the generated lamp power output is applied to a corresponding circle lamp.

A power ratio control output can be determined by using one of the two power ratio control schemes below:

(1) PID power ratio control:

a controlled power for a circle lamp = (PID operation output) \* (corresponding power ratio to the circle lamp),

5 (2) PD-I power ratio control:

a controlled power for a circle lamp = (PD operation output) + ((I operation output) \* (corresponding power ratio to the circle lamp)).

10 The P and the D operation outputs can be greatly varied according to the temperature changes, while the I operation output is less affected by the temperature changes than the P and the D operation outputs. By combining these P, I and D operation outputs properly, the inner temperature of the reaction chamber 102 can reach to a uniform  
15 temperature fast through undergoing a substantially reproducible temperature change process. For instance, when there occurs a temperature change in a wafer loading process, a temperature profile reproducibility can be improved by using a proper combination of P, I, D operation outputs as  
20 will be discussed in further detail hereinafter.

The power ratio determination of step 300 can be carried out as follows. First, by using a dummy wafer or a process wafer, a power output for each of the lamps 0-12 and 0'-12' is controlled by using the lamp controller 20 in such  
25 a way that temperatures detected by the temperature profile sensors on the surfaces of the wafer 103 and/or the

susceptor 106 fall within a predetermined uniform temperature range, e.g., 498°C to 502°C around a corresponding setting temperature, e.g., 500°C. Power output ratios satisfying this condition is set as power ratios for the lamps 0-12 and 0'-12' at the corresponding setting temperature; and at the same time, the temperature(s) sensed by the central temperature sensor 107 and/or the peripheral temperature sensor 108 is recorded and used later as a reference of the setting temperature during an actual device fabrication process.

This procedure is carried out for each of preset different setting temperatures appropriately selected within a temperature range to be used in a device fabrication process. A set of the obtained power ratios for each of the setting temperatures is registered as a power ratio table for that temperature. By using power ratio tables for a selected number of setting temperatures, memory capacity required for the storage thereof can be substantially reduced.

Figs. 4 and 5 are exemplary power ratio tables for the setting temperatures of 500°C and 700°C, respectively. In each table, TBL No. represents a power ratio table number; SV, a setting temperature at which power ratios are obtained; RateH0-12 and RateL0'-12', power ratios corresponding to the upper circle lamps 0-12 and lower circle lamps 0'-12', respectively.

A power ratio table can be selected by designating the table number. In the preferred embodiment of the present invention, however, a programmed power ratio table selection scheme is employed by which a corresponding power ratio  
5 table can be automatically selected according to a control temperature, the control temperature being one of a target temperature and a measured temperature by the central temperature sensor 107 or the peripheral temperature sensor 108.

10 In this method, one or more power ratio tables appropriate to the control temperature are selected among the power ratio tables established and then the power ratio control operation is performed by using the power ratios of the selected power ratio tables. A target temperature or a  
15 measured temperature is adaptively set as a control temperature by considering the temperature reproducibility as will be described in further detail hereinafter.

For instance, if there is one and only power ratio table registered for the single setting temperature of 500°C,  
20 the power ratios of the registered table are used for all control temperatures. If there exist two power ratio tables for the setting temperatures of 500°C and 700°C, linearly interpolated power ratios of the registered power ratios are used for the control temperatures between 500°C and 700°C.  
25 If a control temperature is 800°C, the power ratios of the setting temperature of 700°C can be used for that

temperature without interpolation or the power ratios for 800°C can be obtained by extrapolation based on the power ratios of 500°C and 700°C. The power ratio tables are stored in the NVRAM 205 shown in Fig. 2.

5           Fig. 6 sets forth an exemplary target temperature profile of the wafer 103. Power ratio control operation results carried out with reference to the target temperature profile shown in Fig. 6 based on the power ratio tables shown in Figs. 4 and 5 will be described below. In this  
10       example, it is assumed that the power ratio tables are selected by using target temperatures.

          First, during 0 to 100 seconds, the power ratio table shown in Fig. 4 is used since the target temperature is 500°C. Assuming that P, I and D operation outputs are  
15       respectively 50%, 30% and -10% at the center zone and the PID power ratio control is employed, power ratio control outputs for the circle lamps 0-8 of the upper set 104 and those 0'-7' of the lower set 105 all become 70% ( $=70\%(\text{PID operation output}) * 1.00 \text{ (power ratios)}$ ). When the PD-I power  
20       ratio control is employed, power ratio control outputs for the lamps 0-8 and 0'-7' are also set to be 70% ( $=30\%(\text{I operation output}) * 1.00 \text{ (power ratios)} + 50\%(\text{P operation output}) - 10\%(\text{D operation output})$ ).

          Since the target temperatures are set to increase  
25       between 100 and 200 seconds as set forth in Fig. 6, corresponding power ratios vary with time accordingly. For

instance, if the P, I and D operation outputs are same as above, power ratio control outputs for the target temperature of 600°C at 150 seconds are obtained as follows. The proportional factor of 600°C is  $1/2$   $(=(600-500)/(700-500))$  and PID operation output is  $70\% (= 50\% + 30\% - 10\%)$ .  
5 If the PID power ratio control is employed, the control output of the upper lamp 0 becomes  $70\% (= 70\% * (1.00 + 1.00)/2)$ ; control operation outputs for the upper lamps 1-8 are  $72.1\% (= 70\% * (1.06 + 1.00)/2)$ ; that for the lower lamp 0' is  $70\% (= 70\% * (1.00 + 1.00)/2)$ ; and those for the lower lamps 1'-7' become  $72.1\% (= 70\% * (1.06 + 1.00)/2)$ .  
10

If the PD-I power ratio control is employed, the control outputs for the upper lamp 0 and the lower lamp 0' become  $70\% (= 30\% * ((1.00 + 1.00)/2)) + 50\% - 10\%$ ; and the  
15 control operation outputs for the upper lamps 1-8 and lower lamps 1'-7' become  $70.9\% (= 30\% * ((1.06 + 1.00)/2)) + 50\% - 10\%$ .

Power ratio control outputs for the peripheral zone can be obtained in a similar manner by using P, I, D  
20 operation outputs for the peripheral zone. The PID or PD-I power ratio control scheme can be adaptively employed depending on a state of the apparatus. For example, the PID power ratio control can be preferably used when a temperature is stable or during ramping-up and ramping-down  
25 stages where there is no external disturbance; and the PD-I power ratio control may be preferably employed when there is

an external disturbance due to, e.g., wafer loading and unloading, as will be discussed with reference to Fig. 7.

Referring to Fig. 7, there are illustrated exemplary PID and PD-I power ratio control results obtained in accordance with the preferred embodiment of the present. In Fig. 7, the horizontal axis is a time axis illustrating sequential events of wafer loading, ramp-up, start of a wafer processing, ramp-down, wafer unloading; and the vertical axis represents temperatures.

In Fig. 7, a dotted line S represents target temperatures. The temperatures inside the reaction chamber 102 are basically controlled to follow this target temperature profile. The lines designated by reference signs A1 and A2 represent measured temperature profiles at the center zone obtained by performing the PD-I power ratio control twice; and the lines designated by reference signs B1 and B2 represent measured temperature profiles at the center zone obtained by performing the PID power ratio control twice.

As is apparent from Fig. 7, the PD-I power ratio control provides better reproducibility, i.e., less deviation between A1 and A2, in comparison with a PID power ratio control when an external disturbance, e.g., due to a wafer loading occurs.

An inner temperature of the reaction chamber 102 is greatly changed when there occurs a disturbance due to, e.g.,

gas input or loading of a wafer having a considerable thermal capacity. In this case, P and D operation outputs are greatly affected by the temperature change therein. Since, however, the I operation output is an integration output value, I operation output is affected far less than the P and D operation outputs. Therefore, when a power ratio is multiplied by only the I operation output, the control output can be less affected by the changes of the P and D operation values than in the case where the power ratio is multiplied by all the P, D and I operation outputs.

Accordingly, when an external disturbance occurs, the PD-I power control, wherein a power ratio is multiplied only by the I operation output and this multiplied value is added to the P and D operation outputs, renders the wafer to experience substantially identical temperature profiles, thereby providing better reproducibility of the temperature profile. With the improved reproducibility of the temperature profile, variations of thermal budgets between batches of thermally processed wafers can be decreased, enabling substantially consistent characteristics to be obtained from the films formed on different wafers.

Further it can be seen from Fig. 7 that better temperature response and more stabilized temperature profiles are obtained by using the PID power control scheme when there is no external disturbance, i.e., during the ramp-up and wafer processing stages. Therefore, reliable

and reproducible temperature control can be accomplished by employing the PID power ratio control scheme when there is no external disturbance and the PD-I power ratio control scheme if otherwise.

5 Further, when performing power ratio control in controlling temperatures, a power ratio multiplied by the I operation output can be set to be different from that multiplied by the P and D operation outputs, e.g., by employing appropriate different weighting factors thereto. 10 It is also possible to employ PID power ratio control scheme even when there occurs an external disturbance. In that case, a power ratio multiplied by the I operation output is preferably set to be greater than that for the P and D operation outputs by applying a weighting factor to the 15 power ratio for the I operation output, which is greater than that for the P and D operation outputs.

Referring to Fig. 8, there are depicted two sets of measured temperature profiles obtained by using target temperatures and measured temperatures as the control 20 temperatures being employed for the selection of power ratio tables. In Fig. 8, a dotted line S represents a predetermined target temperature profile; reference signs C1 and C2, two measured temperature profiles at the center zone when the target temperatures are used as the control 25 temperatures; and reference signs D1 and D2, two measured temperature profiles at the center zone when measured

temperatures are used as the control temperatures.

As is apparent from Fig. 8, in the presence of an external disturbance, an improved temperature reproducibility can be obtained when the target temperatures are used as the control temperatures, while setting the measured temperatures as the control temperatures renders the temperature response faster and improves the temperature stability when there exists no or little external disturbances.

In the preferred embodiments described above, there have been presented temperature control processes from a wafer loading stage to a wafer unloading stage in the single wafer epitaxial growth apparatus of the present invention. Fig. 9 presents an exemplary overall process which can be carried out in the single wafer epitaxial growth apparatus of the present invention. Figs. 7 and 8 illustrate a baking stage (S1), a deposition stage (S2) and a wafer unloading stage of the overall process shown in Fig. 9. As presented in Fig. 9, the overall process in the apparatus may further include a chamber cleaning stage (S3).

As exemplified in Fig. 9, a wafer is loaded into the reaction chamber controlled to be at a loading temperature. The loading temperature has an upper limit determined in consideration of the thermal resistance of a wafer carrier and slip generation which might occur in the wafer due to a thermal shock. Subsequently, the wafer is heated upto about

1130°C and a hydrogen baking is carried out to remove an oxide layer and defects from a surface of the wafer. Thereafter, Si epitaxy is performed on the surface of the wafer by CVD using, e.g., trichlorosilane. After depositing a Si epitaxial layer, the reaction chamber is purged with, e.g., a N<sub>2</sub> gas; and the wafer is cooled down to a predetermined unloading temperature and unloaded.

At the subsequent chamber cleaning stage, the reaction chamber is heated to a predetermined elevated temperature to thereby clean impurities deposited on the surface of the susceptor and on the inner wall of the reaction chamber by flowing a HCl gas therethrough. The HCl gas cleaning process is normally carried out for every one to five epitaxial growth processes depending on the overall thickness of corresponding epitaxially grown films. These processes are repeated to produce epitaxially grown wafers to be used as various semiconductor devices.

It should be apparent to those skilled in the art that the temperature controlling method of the invention can be employed in any device fabrication steps, including but not limited to etching, deposition, diffusion, annealing, surface cleaning, oxidation, ramp-up/down and doping, which requires precise temperature control of a substrate. Further, it is to be understood that the inventive temperature controlling method can also be employed in controlling temperatures of a reaction chamber, e.g.,

loading, unloading and chamber cleaning temperatures.

While the present invention has been described with respect to certain preferred embodiments only, other modifications and variations may be made without departing  
5 from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A method for controlling temperatures in a semiconductor manufacturing apparatus including a reaction chamber and a plurality of heating sources, comprising the steps of:

determining a set of power ratios to be fed to the heating sources for each of two or more selected temperatures; and

controlling a given temperature by performing power control on the heating sources based on at least one set of power ratios obtained in the determining step.

2. The method of claim 1, wherein the selected temperatures are discontinuous to have a predetermined temperature interval between every two selected temperatures.

3. The method of claim 1, wherein the power control is carried out by using power ratios for the heating sources corresponding to the given temperature, the power ratios corresponding to the given temperature being determined based on one or two sets of power ratios determined with respect to one or two selected temperatures closest to the given temperature.

4. The method of claim 3, wherein the power ratios corresponding to the given temperature are determined by

interpolating the power ratios of the two sets based on the temperature differences between the given temperature and the two selected temperatures.

5 5. The method of claim 1, wherein said temperature controlling step is carried out by using a P(proportional), an I(integral) and a D(derivative) operation outputs and power ratios corresponding to the given temperature, the power ratios corresponding to the given temperature being  
10 determined based on one or two sets of power ratios determined in the determining step.

6. The method of claim 5, wherein a controlled power output for a heating source is determined by applying a first power  
15 ratio to the I operation output and a second power ratio to the P and the D operation outputs.

7. The method of claim 5, wherein a controlled power output for a heating source is determined by multiplying a power  
20 ratio only by the I operation output.

8. The method of claim 5, wherein a controlled power output for a heating source is determined by multiplying the P, the D and the I operation outputs by a power ratio during  
25 processing a wafer and is determined by multiplying the power ratio only by the I operation output when there exists

an external disturbance in the reaction chamber caused by loading a wafer thereinto.

9. The method of claim 1, wherein said at least one set of  
5 power ratios is selected by using a target temperature.

10. The method of claim 1, wherein said at least one set of power ratios is selected by using a target temperature when there exists an external disturbance in the reaction chamber caused by loading a wafer thereinto and is selected by using  
10 a measured temperature during processing a wafer.

11. The method of claim 1, wherein the reaction chamber includes;  
15 a rotatable susceptor for mounting a wafer thereon;  
a ring die fixedly installed around the peripheral portion of the susceptor; and  
temperature detection devices, for measuring  
temperatures of the reaction chamber, installed near a  
20 center of the wafer and close to a peripheral portion of the wafer.

12. A method for manufacturing a semiconductor device by using the method of claim 1.  
25

13. An apparatus for controlling temperatures by using the method of claim 1.

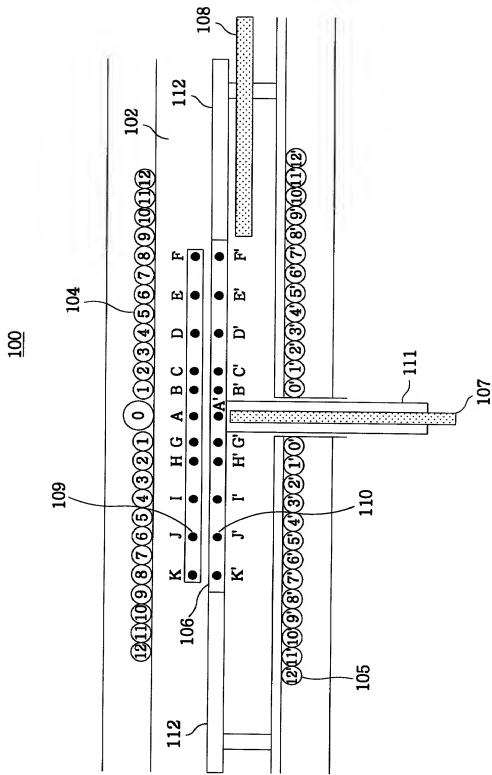
14. An apparatus for manufacturing a semiconductor device  
5 by using the method of claim 1.

# ABTRACT

In a method for controlling temperatures in a semiconductor manufacturing apparatus including a reaction chamber and a plurality of heating sources, a set of power ratios to be fed to the heating sources is determined for each of two or more selected temperatures. Then, a temperature of the reaction chamber is controlled by performing power control on the heating sources based on at least one set of power ratios obtained.

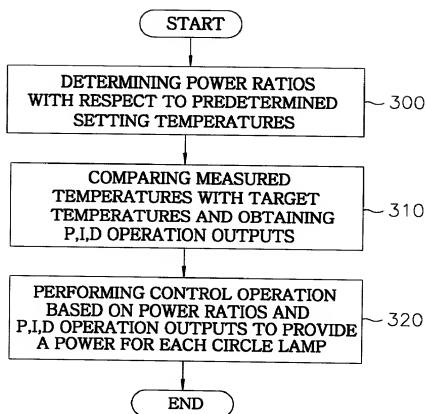


FIG. 1





**FIG. 3**



*FIG. 4*

TBL SV	No.	1
	RateH0-12	0500.0
0	100.0	RateL0'-12'
1	100.0	100.0
2	100.0	100.0
3	100.0	100.0
4	100.0	100.0
5	100.0	100.0
6	100.0	100.0
7	100.0	100.0
8	100.0	100.0
9	100.0	100.0
10	100.0	100.0
11	100.0	100.0
12	100.0	100.0

*FIG. 5*

TBL SV	No.	2
	RateH0-12	0700.0
0	100.0	RateL0'-12'
1	106.0	100.0
2	106.0	106.0
3	106.0	106.0
4	106.0	106.0
5	106.0	106.0
6	106.0	106.0
7	106.0	106.0
8	106.0	115.0
9	110.0	115.0
10	110.0	115.0
11	110.0	115.0
12	110.0	115.0

FIG. 6

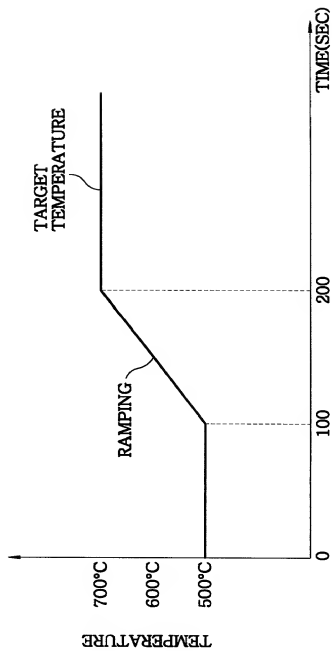


FIG. 7

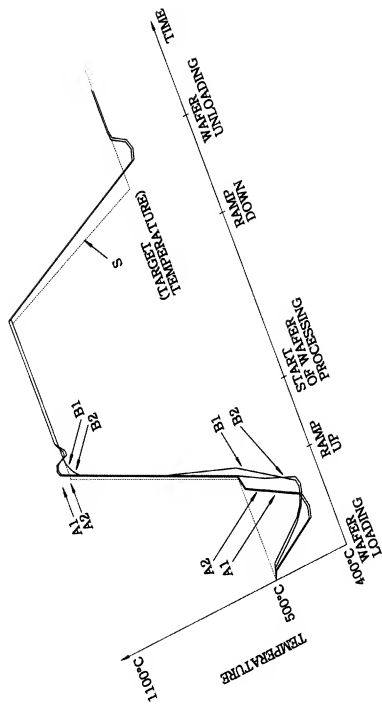
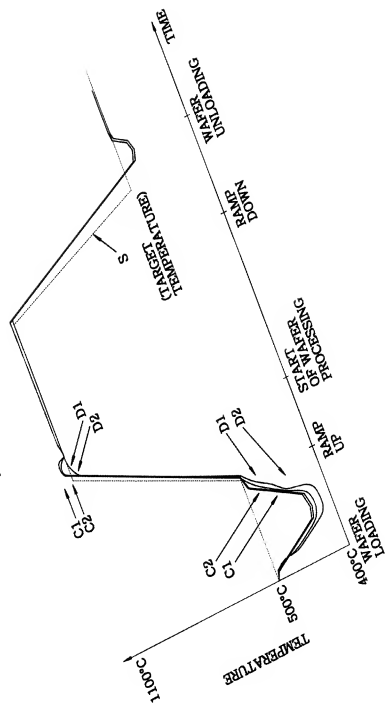
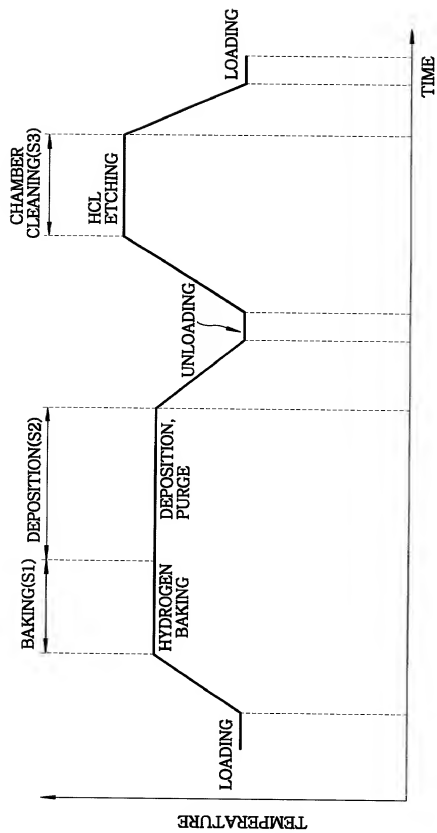


FIG. 8



**FIG. 9**



**ROSENMAN & COLIN LLP  
DECLARATION AND POWER OF ATTORNEY**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below my name,

I believe I am the original, first and sole inventor (if only one name is listed below), or an original, first and joint inventor (if more than one inventor's name is listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD AND APPARATUS FOR CONTROLLING A SEMICONDUCTOR FABRICATION TEMPERATURE**

the specification of which: ☒ [x] is attached hereto ☐ [ ] was filed on \_\_\_\_\_ Title of Invention \_\_\_\_\_ Application Serial No. \_\_\_\_\_  
(for declaration not accompanying application)

with amendment(s) filed on \_\_\_\_\_  
(date(s) of all amendments)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/§172 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (Day, Month, Year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119/172
2000-019934	Japan	28, 01, 2000	Yes <input checked="" type="checkbox"/> X No
			Yes _____ No
			Yes _____ No

I hereby claim the benefit under Title 35, United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint Shahan Islam (Reg. No. 32,507) whose address is **Rosenman & Colin LLP**, 575 Madison Avenue, New York, New York 10022-2585 as my attorney, to prosecute this application, and to transact all business in the U. S. Patent and Trademark Office connected therewith.

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Home Address	No. and Street Address <b>14-20, 3-chome, Higashi-Nakano, Nakano-ku</b>	City <b>Tokyo</b>	State or Country <b>Japan</b>		Zip Code <b>164-8511</b>
Full Name of 4th Inventor	Last Name		First Name		Middle Name
Residence & Citizenship	City	State or Foreign Country		Country of Citizenship	
Home Address	No. and Street Address	City	State or Country		Zip Code

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of 1st Inventor <i>Minoru Nakano</i>	Signature of 2nd Inventor <i>Masaaki Ueno</i>	Signature of 3rd Inventor <i>Kazuo Tanaka</i>	Signature of 4th Inventor
Date <i>September 20, 2000</i>	Date <i>September 20, 2000</i>	Date <i>September 20, 2000</i>	Date